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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,324	08/20/2003	Brian Johnson	2269-4196.1US (99-0458.01	6644

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EXAMINER	
BRAGDON, REGINALD GLENWOOD	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,324	JOHNSON, BRIAN	
	Examiner	Art Unit	
	Reginald G. Bragdon	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-13 and 16-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-13 and 16-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 11-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Camilleri et al. (6,389,490).

As per claim 11, Camilleri et al. teaches, with reference to figures 1 and 2, a FIFO buffer 101, a write address register 220 ("write counter") and a read address register 210 ("read counter"). The read address register includes a "last read address register" 216 ("at least one pointer register configured to maintain a previous read counter setting") and a "current read address register" 214 ("during a current reading from the FIFO"). See also column 7, lines 32-43. The entire FIFO circuit 100 (including the buffer 101 and flag control 107, which includes the read and write address registers) is implemented by a field programmable gate array (FPGA), which is a "semiconductor substrate"

As per claim 12, the FPGA is implemented on a "semiconductor wafer".

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4, 6, and 17-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hang (5,487,049) in view of Camilleri et al. (6,389,490).

As per claim 1, Hang teaches, with respect to figure 1, a DRAM 16, a DRAM controller for controlling the DRAM (see column 4, line 30), and a FIFO 10 associated with the DRAM (see column 2, lines 60-63). Hang further teaches at column 3, lines 63-67, that the data register 30 and address register 34 are two-port memories which can simultaneously write data to a storage location having an address specified by a write count value while reading data from a different storage location having an address specified by a read count value. The claimed "control logic" is represented, at the least, by write counter 22, read counter 26, and state machine 20, as shown in figure 1.

Hang teaches that the state machine generates a "full" signal and an "empty" signal. See column 2, lines 30-37, and column 3, lines 35-41. However, Hang does not teach "at least one read counter associated with the FIFO and configured to maintain a previous read counter setting of the read counter during a current reading from the FIFO".

Camilleri et al. teaches, with reference to figures 1 and 2, a FIFO buffer 101 and a read address register 210 ("read counter"), where the read address register includes a "last read address register" 216 ("at least one pointer register configured to maintain a previous read

counter setting") and a "current read address register" 214 ("during a current reading from the FIFO"). See also column 7, lines 32-43. In order to determine whether the a buffer is full, the write counter value is compared to the last used ("previous") read counter value (column 3, line 65-67), as opposed to the prior art described by Camilleri et al. (and similar to the system of Hang et al.), where in order to determine if a buffer is full, the write counter is compared to the current read counter value.

It would have been obvious to one of ordinary skill in the art to have modified Hang to include a last used ("previous") address counter register, as suggested by Camilleri et al., because Camilleri et al. teaches that the inclusion of a last used address register would simplify the determination of the full and empty conditions, thereby providing a reliable and robust structure and method of controlling a FIFO memory system. See column 4, lines 1-7.

As per claim 4, Hang teaches a write counter 22 associated with the FIFO.

As per claim 6, Hang teaches a FIFO system 10 including a FIFO data buffer 30 and address buffer 34, a write counter 22, and a read counter 26. See figure 1. The claim is further rejected for the reasons set forth for claim 1, above.

As per claim 17, Hang teaches, with respect to figure 1, a DRAM 16, a DRAM controller for controlling the DRAM (see column 4, line 30), and a FIFO 10 associated with the DRAM (see column 2, lines 60-63). A memory address is transmitted over address bus (ADRBUS) 12 ("receiving at least one memory bank address command bit") and written to the address register 34 ("writing the at least one memory bank address command bit to the at least one FIFO buffer"). See column 3, lines 15-16, and column 4, lines 20-21. Data is received over DBUS 14 ("receiving data corresponding to the at least one memory bank address command bit at the

control logic"). See column 4, lines 17-19. The memory bank address is read ("reading the memory bank address command") and the associated data is then written to the DRAM ("storing the data..."). See column 4, lines 23-29. The claim is further rejected for the reasons set forth above for claim 1.

As per claim 18, Hang teaches a write counter 22. A write pointer signal ("write latch signal"), WPTRN, is received by the write counter ("transmitting a first write latch signal..."), which causes the write counter to increment and point at another slot to be filled during a write operation ("adjusting the write counter..."). See column 3, lines 29-32.

As per claim 19, Hang teaches at column 4, lines 4-6, that WCNT increases in value from an initial value of 00. Therefore, the write counter is reset to a value of 00 prior to beginning the count.

As per claim 20, Hang teaches a FIFO buffer. Inherently a second memory bank address command will be received along with corresponding data, which will be read from the FIFO using the stored address for storage in the DRAM, in a manner similar to the first memory bank address command that is received.

As per claim 21, Hang teaches, with reference to figure 2, a plurality of sequential FIFO buffers, a write counter WCNT, and a read counter RCNT. The write counter is always maintained pointing ahead of the read counter. See figure 2 and column 4, lines 36-39.

As per claim 22, Hang teaches a write counter 22. A write pointer signal ("write latch signal"), WPTRN, is received by the write counter, which causes the write counter to increment and point at another slot to be filled during a write operation, prior to the read counter incrementing. See column 3, lines 29-32.

As per claim 23, Hang teaches a FIFO buffer having read counter 26 and write counter 22, which both initially point "00". A first data word is received and stored in the FIFO buffer. See column 4, lines 17-21. The write pointer is then incremented ("adjusting the write counter…). See column 4, lines 4-6, and 17. The write counter is maintained pointing ahead of the read pointer. See column 4, lines 36-39. The claim is further rejected for the reasons set forth for claim 1, above

As per claim 24, Hang teaches reading the data from the FIFO buffer for storage in the DRAM as set forth in column 4, lines 23-29.

As per claim 25, Hang teaches a page in, burst-out FIFO buffer 10 (figure 1) that includes an address register 34 (" temporarily storing…address command) and a data register 30 ("receiving" and "storing" data). See in general figure 1. Hang teaches a FIFO buffer. Inherently a second memory bank address command will be received along with corresponding data, which will be read from the FIFO using the stored address for storage in the DRAM, in a manner similar to the first memory bank address command that is received. Hang sets forth that the address register FIFO 34 which holds 8 column addresses previously stored associated with data that is to be stored in the data register 30 and DRAM 16. See column 3, lines 62-67, and column 4, lines 26-29. Hang also teaches, with reference to figure 2, a plurality of sequential FIFO buffers, a write counter WCNT, and a read counter RCNT. The write counter is always maintained pointing ahead of the read counter. See figure 2 and column 4, lines 36-39. The claim is further rejected for the reasons set forth for claim 1, above.

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hang in view of Camilleri et al. in further view of Rust et al. (5,699,530).

As per claim 7, the combination of Hang and Camilleri et al. does not teach that the counter registers are linear feedback shift registers. Rust et al. teaches that it was know in utilize linear feedback shift registers for read/write pointers in FIFO buffers. See the abstract at the bottom. It would have been obvious to one of ordinary skill in the art to have modified the counter registers of Hang and Camilleri et al. to utilize linear feedback shift registers, as suggested by Rust et al., because Rust et al. teaches that linear feedback shift registers are advantageous in reducing the propagation time for selection signals traveling to an actual storage location. See column 3, lines 20-24.

6. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hang in view of Camilleri et al. in further view of Thome et al. (5,289,584).

As per claims 8 and 10, the claims are rejected for the reasons set forth for claim 6, above, further noting:

Hang does not specifically mention a processor, input device (e.g. keyboard or mouse), output device (e.g. monitor), and a storage device (e.g. disk drive, tape drive). Thome et al. teaches a system including a page mode DRAM and a FIFO 114 or 116 (figure 2), which includes a CPU 30, keyboard 80 ("input device"), monitor 64 ("output device") and a hard disk 98 ("storage device"). See figure 1. It would have been obvious to one of ordinary skill in the art to have included a processor, input device, output device, and a storage device attached to the system bus disclosed at column 2, lines 50-51, because these elements are well known components of a computer system for the processing of data, storage of data and interaction with a user.

As per claim 9, Hang teaches that the memory device is a DRAM 16.

7. Claims 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hang in view of Camilleri et al. in further view of Wu et al. (6,329,997).

As per claims 13 and 16, the combination of Hang and Camilleri et al. teaches the invention as set forth above for claim 1. However, Hang does not teach that the FIFO is embodied on a semiconductor substrate (semiconductor wafer) with the DRAM. Wu et al. teaches that it was known to incorporate a FIFO on the same substrate with a DRAM. See column 3, lines 8-20. It would have been obvious to one of ordinary skill in the art to have incorporated a FIFO with a DRAM on a single semiconductor substrate/wafer, as suggested by Wu et al., because this simplifies production of the system, thereby saving cost, as well as reducing the distance between functional elements, realizing an improvement in speed as well as a reduction in power.

Response to Arguments

8. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection necessitated by Applicant's amendments to the claims.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any response to this final action should be mailed to:

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

All "OFFICIAL" patent application related correspondence transmitted by FAX must be directed to the central FAX number at **(571) 273-8300**:

"INFORMAL" or "DRAFT" FAX communications may be sent to the Examiner at **(571) 273-4204**, only after approval by the Examiner.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (571) 272-4204. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (571) 272-4210.

RGB
August 31, 2005

Reginald G. Bragdon
Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188